What is claimed is:

1. An integrated circuit memory device comprising:

a semiconductor substrate;

a plurality of word line structures on predetermined portions of the semiconductor substrate;

word line contact plugs, each of which is disposed between adjacent word line structures;

storage node contact plugs in electrical contact with predetermined ones of the word line contact plugs;

storage node electrodes on the storage node contact plugs; and

a plate electrode between the storage node electrodes and between the storage node contact plugs.

2. The integrated circuit memory device of claim 1, wherein the plate electrode extends between lower portions of the storage node contact plugs.

3. The integrated circuit memory device of claim 1, further comprising a plate insulating layer between the plate electrode and the storage node contact plugs that insulates the plate electrode from the storage node contact plugs.

4. The integrated circuit memory device of claim 1, wherein the storage node electrodes are directly on the storage node contact plugs.

5. The integrated circuit memory device of claim 1, wherein the word line structures each comprise a gate electrode, a gate insulating layer insulating the gate electrode from the semiconductor substrate, and an insulating material covering a top surface and sides of the gate electrode.

6. An integrated circuit memory device, comprising:

a semiconductor substrate;

a pair of spaced apart word line structures on the substrate;

an interlayer insulating layer on the word line structures;

a bit line structure on the interlayer insulating layer that is transverse to the word line structures;

a first capacitor electrode that extends from the substrate between adjacent word line structures, through the interlayer insulation layer, and beyond the bit line structure;

a capacitor dielectric on the first capacitor electrode and directly on the bit line structure; and

a second capacitor electrode on the capacitor dielectric.

7. The memory device according to Claim 6, wherein the capacitor dielectric is directly on the interlayer insulation layer.

8. An integrated circuit memory device comprising:

a semiconductor substrate;

a plurality of word line structures on predetermined portions of the semiconductor substrate;

word line contact plugs between adjacent word line structures;

bit line structures in electrical contact with a first set of the word line contact plugs;

storage node contact plugs on, and electrically connected to, a second set of the word line contact plugs that is different from the first set of the word line contact plugs;

storage node electrodes on the storage node contact plugs;

a dielectric layer on the storage node contact plugs and the storage node electrodes; and

a plate electrode on the dielectric layer and between the storage node contact plugs and between the storage node electrodes.

9. The integrated circuit memory device of claim 8, wherein the plate electrode is between lower portions of the storage node contact plugs.

10. The integrated circuit memory device of claim 8, wherein the storage node contact plugs are directly on the second set of the word line contact plugs.

11. The integrated circuit memory device of claim 8, wherein the storage node contact plugs are directly on the bit line structures.

12. The integrated circuit memory device of claim 8, wherein the storage node electrodes are directly on the storage node contact plugs.

13. the integrated circuit memory device of claim 8, wherein the dielectric layer is directly on the bit line structures.

14. The integrated circuit memory device of claim 8, wherein:

the word line structures each comprise a gate electrode, a gate insulating layer which insulates the gate electrode from the semiconductor substrate, and an insulating material on a top surface and sides of the gate electrode, and

the bit line structures each comprise a bit line and a dielectric layer on a top surface and sides of the bit line.